REMARKS

Claims 1-3 are pending. By this Amendment, the specification and claim 1 have been amended. Reconsideration and allowance are respectfully requested in view of the above amendments and the following remarks. No new matter is believed added.

Claims 1-3 are rejected under 35 U.S.C. §102(b) as being anticipated by Hawkins et al. (US 5,641,700), hereafter "Hawkins." This rejection is defective because Hawkins fails to teach each and every feature of the claims as required by 35 U.S.C. §102.

Regarding claim 1, Hawkins fails to teach, among other features, the formation of semiconductor regions in a silicon slice, wherein the "semiconductor regions are not formed in the silicon slice until after the gate dielectric has been provided on the surface of the silicon slice, the ions of the dopants being implanted through the gate dielectric, and wherein the system of electrodes is formed on the gate dielectric after the formation of the semiconductor regions." On the contrary, Hawkins forms conductive electrodes 40 **prior** to forming biasing implant 44 (see e.g., FIG. 2G and 2H). In particular, Hawkins discloses that "it is required that alignment of a second charge transfer direction biasing implant be made at the left sides of the conductive electrodes 40" (col. 7, lines 21-34) prior to the formation of the biasing implant 44. Indeed, the electrodes 40 are used in combination with photoresist layer 42 to define the width of the biasing implant 44. Clearly, Hawkins does not disclose forming the system of electrodes 40, 50, **after** the formation of the biasing implants 34 and 44 as set forth in claim 1. According, Applicants request withdrawal of the rejection of claims 1-3 under 35 U.S.C. §102(b).

Accordingly, Applicants respectively submit that claims 1-3 are in condition for

allowance.

If the Examiner believes that anything further is necessary to place the application in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number listed below.

Respectfully submitted,

Dated: 12/11/02

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DOCKET NO. PHNL000359

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Peek et al.	)	Examiner: Fourson, G.
Application No.: 09/888,463	)	Art Unit: 2823
Filed: 06/25/2001	)	
For: Method of Manufacturing a Charge-Coupled Image Sensor	)	

Box Non-Fee Amendment
Commissioner for Patents
Washington D.C. 20231

SEPARATE MARKUP SHEET

In the Specification

Please amend the paragraph starting on page 4, line 12 as follows:

As shown in Fig. 5, after the formation of the p-well 8 on the gate dielectric 3, 4, a photoresist mask 9 is formed comprising strips of photoresist 10 extending transversely to the plane of the drawing. This photoresist mask 9 is used to define n-type channels to be formed in the p-well 8. After the formation of the photoresist mask 9, phosphor ions, indicated by means of dashed lines 11, are implanted in the slice 1. After the removal of the photoresist mask 9, the slice is subjected to a thermal treatment wherein the n-type channel zones 12, shown in Figs. 1 and 6, are formed. Centrally below these channels, the p-well [9] 8 has a smaller thickness. In Fig. 1, the channel regions 12 are shown in a plan view indicated by means of dashed lines.

Please amend the paragraph starting on page 4, line 21 as follows:

After the formation of the n-type channels 12, the gate dielectric 3, 4 is provided, as shown in Fig. 7, with a next photoresist mask 13 comprising strips of photoresist 14 extending transversely to the plane of the drawing. Said photoresist mask [14] 13 serves to define, in the p-well 8, the channel-stop regions separating the n-type channels 12 from each other. After the formation of the photoresist mask 13, boron ions, indicated by means of dashed lines 15, are implanted in the slice 1. After the removal of the photoresist mask 13, the slice is subjected to a thermal treatment wherein the p-type channel-stop regions 16, as shown in Figs. 1 and [7] 8, are formed. The channel-stop regions 16 indicated by means of dashed lines are also shown in a plan view in Fig. 1.

Please amend the paragraph starting on page 4, line 32 as follows:

After the formation of the semiconductor regions 8, 12 and 16, an approximately 500 nm thick n-type conductive layer of polycrystalline silicon [14] is deposited in a customary manner on the gate dielectric 3, 4, a first system of electrodes 17 being etched in said polycrystalline silicon layer. These electrodes are provided with an insulating layer of thermally formed silicon oxide 18. By virtue of the presence of the silicon nitride layer 4, a mask is not necessary to carry out the oxidation process. The whole is subsequently covered with a silicon nitride layer 19. A plan view of the electrodes 17 is shown in Fig. 1.

In the Claims

Please amend claim 1 as follows:

1. (Amended) A method of manufacturing a charge-coupled image sensor, wherein semiconductor regions are formed in a silicon slice so as to adjoin a surface thereof by implantation of ions of dopants and subsequent thermal treatments, wherein the surface of the silicon slice is provided with a gate dielectric comprising a layer of silicon oxide and a silicon nitride layer deposited thereon, and wherein a system of electrodes is formed on the gate dielectric, characterized in that the semiconductor regions are not formed in the silicon slice until after the gate dielectric has been provided on the surface of the silicon slice, the ions of the dopants being implanted through the gate dielectric, and wherein the system of electrodes is formed on the gate dielectric after the formation of the semiconductor regions.